REMARKS

The subject application is a divisional of U.S. Serial No. 09/074,078, filed May 7, 1998. The subject application also claims the benefit of priority from Japanese Application No. 9-137813, filed May 12, 1997.

By this Preliminary Amendment, Applicant has canceled claims 1-12 and 15, and amended claims 13 and 14. Accordingly, claims 13 and 14 are now pending and presented for examination in the subject application.

Applicant maintains that this Preliminary Amendment does not introduce new matter. Accordingly, Applicant respectfully requests entry of this Preliminary Amendment.

If a telephone interview would be of assistance in advancing prosecution of the subject application, Applicant's undersigned attorney invites the Examiner to telephone him at the telephone number provided below.

No fee, other than the $750.00 application fee for the divisional application filed concurrently herewith, is deemed necessary in connection with the filing of this Preliminary Amendment. However, if any additional fee is required, authorization is hereby given to charge the amount of any such fee to Deposit Account No. 03-3125.

Respectfully submitted,

Paul Teng, Reg. No. 40,837
Attorney for Applicant
Cooper & Dunham LLP
1185 Avenue of the Americas
New York, New York 10036
(212) 278-0400

COPY SHOWING THE CHANGES BEING MADE TO THE CLAIMS

Please amend claims 13 and 14 as follows, by deleting the matter shown by strikethrough and inserting the underlined matter:

13. (Amended) A method of fabricating a semiconductor device comprising ~~a mount substrate; a high frequency transmission line provided on a top surface of said mount substrate; a semiconductor chip mounted on said top surface of said mount substrate in a facedown state in electrical contact with said high frequency transmission line, said semiconductor chip thereby having a bottom surface facing said top surface of said mount substrate; and a depression formed on said top surface of said mount substrate, said semiconductor chip carrying an air bride structure on said bottom surface~~ a silicon substrate carrying a ground plane, a dielectric layer provided on said ground plane, a signal layer provided on said dielectric layer, a depression formed in said dielectric layer so as to extend down to said substrate through said signal layer and said ground plane, and a semiconductor chip carrying thereon an air bridge structure, said semiconductor chip being flip chip mounted onto said silicon substrate, said method comprising ~~a~~ the steps of:

forming said depression in said silicon substrate by an etching process ~~to said top surface of said mount substrate~~; and

mounting said semiconductor chip on said ~~mount~~ silicon substrate such that said air bridge structure is accommodated into said depression.

14. (Amended) A method as claimed in claim 13, wherein ~~said mount substrate is formed of Si, and wherein~~ said etching step includes ~~an anisotropic~~ a wet etching process applied to said ~~top surface of said mount~~ silicon substrate.